

A New 'T' Circuit Topology for the Broadband Modelling of Symmetric Inductors Fabricated in CMOS Technology

Willam Tatinian[†], Philippe Pannier[†], Renaud Gillon[‡]

([†]) Institut Charles Fabry, Marseille, France.

([‡]) Alcatel Microelectronics, Westerring 15, B-9700 Oudenaarde, Belgium

Abstract - This paper shows that the conventional P-type model is not suitable for the broadband modelling of symmetrical inductors. A T-shaped model topology is introduced and a suitable extraction procedure is proposed for its parameters. The new model allows to reproduce the measured behaviour of symmetric inductors up to twice the self-resonance frequency.

I. INTRODUCTION

Today system-on-chip solutions are being designed in deep-submicron CMOS technologies for consumer-market HF applications like 'BlueTooth'. The voltage-controlled oscillator (VCO) is a critical part of the transceiver. Its design amounts to find the correct trade-off between power consumption and phase-noise, which is complicated by the fact that the VCO performance has a strong impact on the quality of the radio link and on the total power budget of the chip. Accurate simulation of the VCO behaviour is hence a must. In particular, due to the large-signal operation of the device, harmonic signals are likely to be generated and it is important that models not only cover the working frequency range but also frequencies up to several harmonics. This paper focuses on the broadband modelling of inductors for use in VCO's.

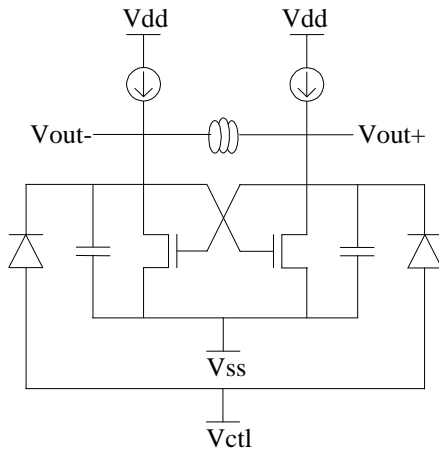


Figure 1 : VCO circuit schematic

II. MODELS FOR SYMMETRIC INDUCTORS

A typical VCO configuration is shown in Figure 1. In such a circuit, the inductor is fed with differential signals and it is important to avoid conversion of signals to common-mode that increases the losses of the oscillator and eventually perturbs differential circuits fed by the VCO. The symmetric inductor design proposed in [1] is therefore used, where at each half turn the track jumps one position inward or outward (Figure 2). We designed a test-chip containing such inductors, that was fabricated in a standard 0.25 μm CMOS process with 5 metallisation levels on 20 $\Omega\text{ cm}$ material. S-parameters were measured on-wafer and in-situ TRL calibration was used for de-embedding.

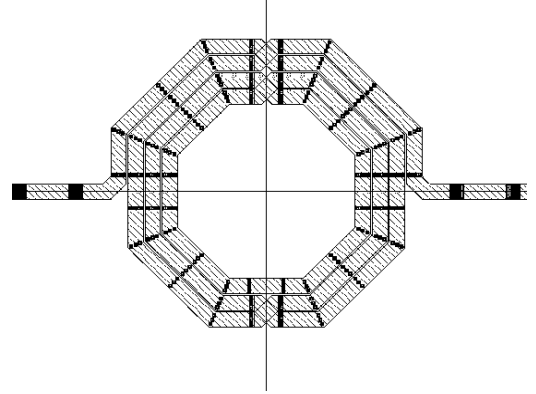


Figure 2 : Symmetric inductor layout

We first extracted parameters for the conventional Π -type equivalent circuit model (Figure 3) used by many authors, [2]-[4]. We show in Figure 4 that this equivalent circuit can not reproduce the phase of the measured transadmittances Y_{21} and Y_{12} around the self-resonance as it goes in the range between -90° and $+90^\circ$ where the real parts of the transadmittances are positive. To overcome this limitation of the conventional Π -type model, we introduce a new type of equivalent circuit using a T-shaped topology as shown in Figure 5.

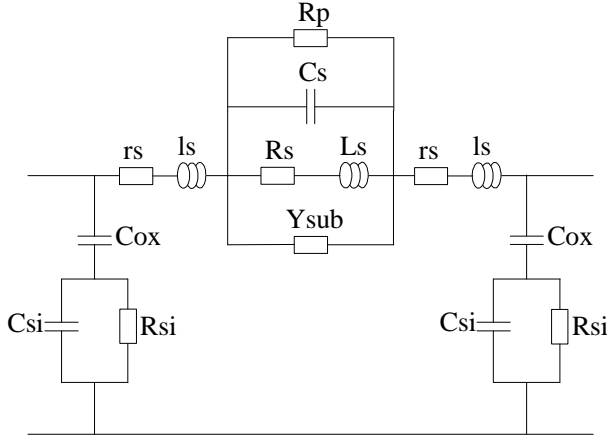


Figure 3 : Conventional Π-model.

III. EXTRACTION PROCEDURE

We developed an appropriate extraction procedure for the new model, based on the analysis of the differential- and common-mode admittances of the inductors, computed according to the following definitions in term of the port voltages and currents, $V_k, I_k, k \in \{1,2\}$:

$$\begin{aligned} I_{Diff} &= \frac{1}{2}(I_1 - I_2) & I_{Com} &= (I_1 + I_2) \\ V_{Diff} &= (V_1 - V_2) & V_{Com} &= \frac{1}{2}(V_1 + V_2) \end{aligned} \quad (1)$$

Our T-shaped model lends itself very well to this kind of analysis, as a natural separation between the substrate network and the metallisation network occurs : In differential mode, the central node of the circuit behaves like a virtual ground and the substrate network is not excited; In common-mode the shunt capacitor of the metallisation network sees no excitation, and extraction can focus on the substrate network.

A. Differential-mode characteristics

Extraction of the circuit parameters for the metallisation network from the differential characteristics shown in Figure 6 is fairly straightforward. The total inductance $(L+l)$ and the resistance R are extracted from the low-frequency limit of the measured curves. The inter-turn and cross-over capacitance C is then estimated from the first self-resonance, whilst the ratio of the first and second resonances gives a hint about the ratio of the inductances L and l . The second resistor r allows to get a correct quality factor for the second self-resonance. A final tuning of all values is then performed, making sure that the fit between measured and simulated

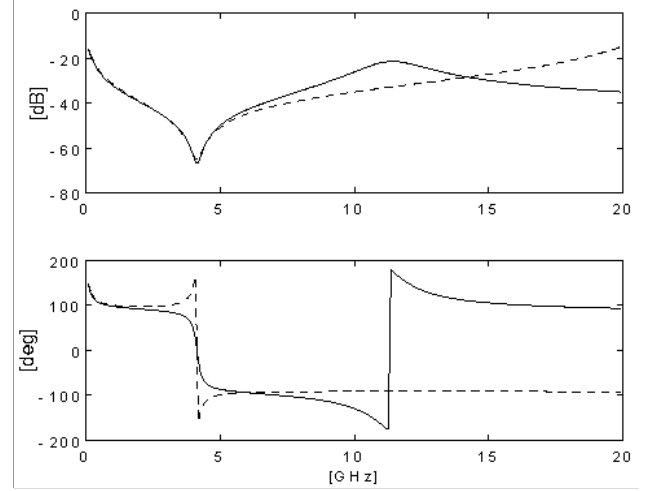


Figure 4 : Measured transadmittance (full line) and Π-model (dashed line)

characteristics degrades gracefully towards higher frequencies.

B. Common-mode characteristics

The common-mode characteristics are somewhat more complicated to analyse (Figure 7). As the currents in neighbouring tracks are flowing in opposite directions, magnetic coupling in common-mode is different : the mutual inductance is subtracting from the self inductance, instead of adding up as in differential mode, [5]. Furthermore, in common-mode, the average magnetic field experienced by each track is much less than in differential mode [6], especially for the inner turns. As a result, losses due to current-crowding in the tracks is much reduced in common-mode, and hence the apparent resistance is smaller than for a differential excitation.

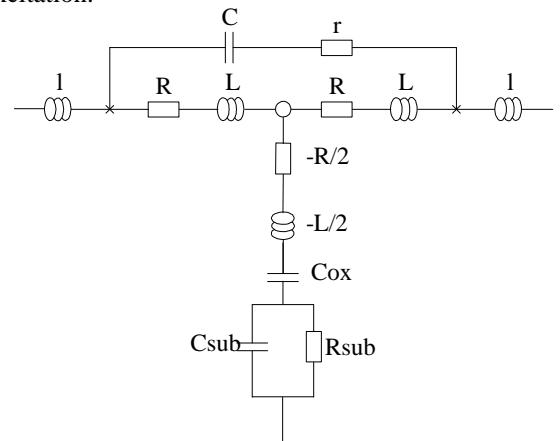


Figure 5 : T-type model

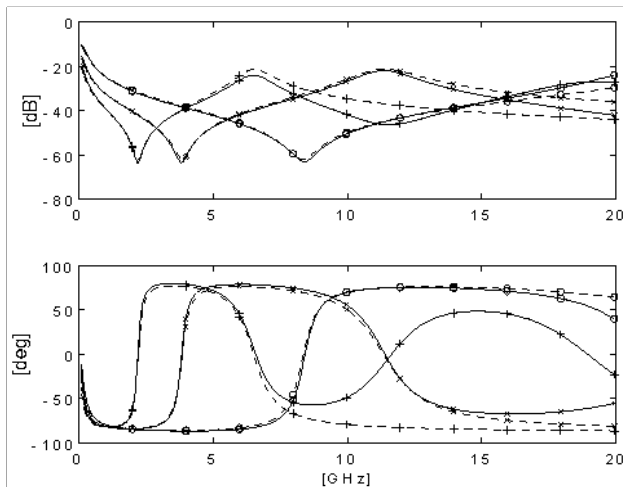


Figure 6 : Differential-mode admittance for 3 inductors (dashed line : model; continuous line : measurements).

To account for the decrease of the apparent inductance and resistance in common-mode, negative inductance and resistance values are added in series with the substrate-network. These negative values are chosen simply as a quarter of the total series inductance and resistance present in the metallisation network.

IV. RESULTS

In spite of their simplicity, the resulting models reproduce the behaviour of the inductors very well , both for differential-mode and common-mode characteristics, and in a band stretching up to twice the self-resonance frequency (Figure 6Figure 7). As shown in Figure 8, even the quality factor is very well reproduced. The extent of the valid frequency range, the simplicity of the extraction and the physical insight gained from it are unique features of our approach based on T-type topology and analysis of differential and common-mode characteristics.

V. CONCLUSION

We showed in this paper that the conventional Π -type model is not suitable for the broadband modelling of symmetrical inductors. We introduced the T-shaped model topology and proposed an extraction procedure for its parameters. We were also able to provide a physical interpretation for all model parameters. Our new model allows to reproduce the measured behaviour up to twice the self-resonance frequency.

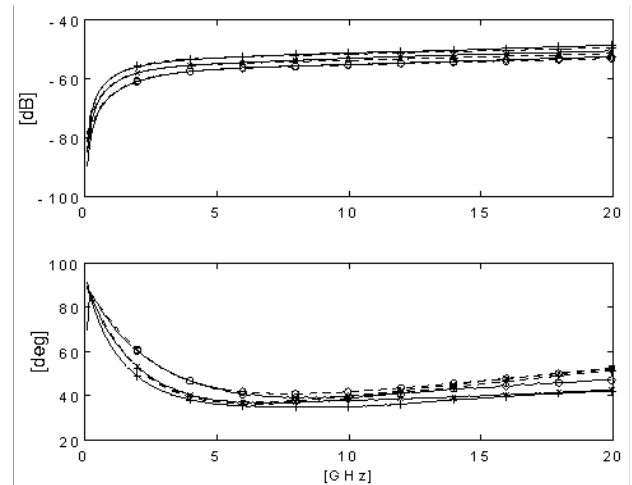


Figure 7 : Common-mode admittance for 3 inductors (dashed line : model; continuous line : measurements)

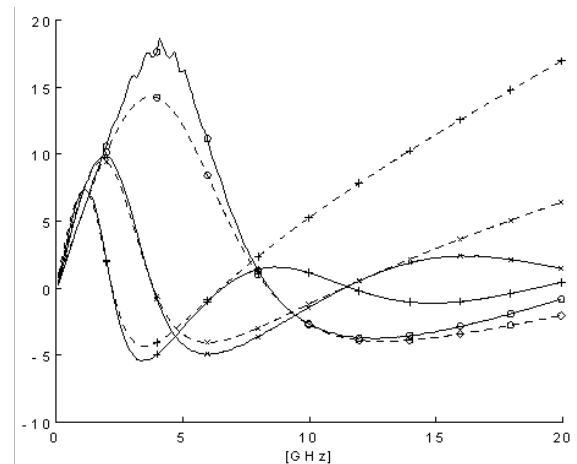


Figure 8 : Differential mode apparent Q-factor (dashed line : model; continuous line : measurements)

REFERENCES

- [1] J. Craninckx, M. Steyaert, Low-noise voltage-controlled oscillators using enhanced LC-tanks, in IEEE Transactions on Circuits And Systems, vol. 42, no. 12, pp. 794-804, December 1995.
- [2] J. R. Long, M. A. Copeland, "The modelling, characterization, and design of monolithic inductors on silicon RF IC's", IEEE Jour. SSC, Vol. 32, No 3, pp. 357-368.
- [3] C. Yue et al. , "A physical model for planar spiral inductors on silicon", IEDM'96,p. 155, 1996.
- [4] C. P. Yue, S. S. Wong, "Physical Modeling of Spiral Inductors on Silicon", IEEE Trans. ED, Vol. 47, No. 3, Mar. 2000, pp. 560-568.
- [5] Y. K Koutsoyannopoulos, Y. Papananos, " Systematic Analysis and Modelling of Integrated Inductors and

Transformers in RF IC Design", IEEE Trans. CAS-II, Vol 47, No. 8, August 2000.

- [6] J. M. López-Villegas et al., “Improvement of the Quality Factor of RF Integrated Inductors by Layout Optimisation”, IEEE Trans. MTT, Vol. 48, No. 1, Jan 2000, pp. 76-83.
- [7] M. Park et al., “Frequency-Dependent Series Resistance of Monolithic Spiral Inductors”, IEEE MGWL, Vol. 9, No. 12, Dec. 1999, pp. 514-516.